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Report 10448
Final Resubmittal
November 1994

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Earth Observing System (EOS)/ Advanced Microwave Sounding Unit-A (AMSU-A) Instrument Logic Diagrams

Contract No: NAS 5-32314
CDRL: 302

Submitted to:

National Aeronautics and Space Administration
Goddard Space Flight Center
Greenbelt, Maryland 20771

Submitted by:

Aerojet
1100 West Hollyvale Street
Azusa, California 91702

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EOS/AMSU-A-CDRL INSTRUMENT LOGIC DIAGRAMS

1. Scope

1.1 Description

This document consists of a set of block diagrams and internal logic diagrams that show the signal inputs, outputs, and internal signal flow.

2. Description

2.1 Functional Block Diagrams, Figures 1 and 2, show the signal flow in the AMSU-A instrument and the general interface to the spacecraft. Each major subfunctition is described in the following paragraphs. Passive analog circuits include sensors on the receiver shelves, warm loads, and drive motors.

2.2 Signal Processor and Power Distribution Block Diagrams, Figures 3 and 4, provide the next level of detail and show the division of functions in the analog processor. Radiometric data processed in the analog processor into multiplexed parallel digital form and delivered to the digital processor where they are packetized and formatted in preparation for transmission via the MIL-STD-1553 interface. Temperature and other analog engineering data are submultiplexed and join the data stream at the analog multiplexer/digitizer. Digital engineering data are fed directly to the digital processor after appropriate conditioning. The digital processor generates all necessary timing pulses and data for the instrument, including clock pulses to the DC/DC converter.

2.3 The Analog Processor Block Diagram, Figure 6, provides a more detailed diagram of signal flow and functions within the analog processor. For the purposes of this diagram, no differentiation is made between the A1 and A2 instrument modules. Radiometric signals from the receiver are detected in the Detector/Preamplifier assembly where they generate a low-frequency output, typically between 0 and 2.0 volts. There are 13 channels in the A1 module and 2 in the A2. The detected signals are integrated and the integrated values fed to the multiplexer where they are sampled and placed in a serial stream. After each sample period, the integrator is reset by the "dump" pulse. The serial analog data stream is digitized in the A/D converter into a 15-bit parallel output that enters the instrument local computer bus via an I/O port on the Timing and Control circuit card assembly (CCA). All multiplexer address and other timing data are generated by the Timing and Control CCA.

Temperature data take two forms; high precision from the warmloads and medium precision from diagnostic sensors spread throughout the instrument. These data are submultiplexed into three groups in conjunction with already multiplexed engineering data and two reference voltages, then delivered to three inputs of the radiometric data multiplexer described above. There they are processed in the same way as the radiometric data and join the data stream to the digital processor.

Engineering data arrive in both analog and digital form at the multiplexer/relay CCA. Digital data enter the local computer bus directly via an input/output (I/O) port, while the analog data are voltage normalized and multiplexed for transmission to the temperature sensor analog mux described above. The Mux/Relay CCA carries some power switching relays and their status is also transmitted to the digital processor via the I/O port for inclusion into the engineering data stream.

2.4 Digital Processor Block and Logic Diagrams, Figures 6 through 12, show the configuration of the EOS/AMSU-A digital processor. The processor is controlled by the central

The Timing and Control CCA generates all timing and address signals for use by the instrument. The Scan Control Interface CCA sends position commands to and receives position data from the antenna drive subsystem. The Mux/Relay CCA has already been described under the Analog Processor section above and is included because it serves both digital and analog functions. The MIL-STD-1553 interface receives commands and timing data from the spacecraft and transmits science, engineering, and diagnostic data.

2.5 Scan Drive Electronics Block Diagrams, Figures 13 and 14, show the signal paths from the Digital Processor through the Scan Drive Subsystem. Antenna position data are stored in the PROM in the Digital Processor. These data are strobed into the Drive Electronics where they are compared with the current antenna position in a digital subtractor. The 14-bit digital error signal is converted into analog form and processed through a triple notch filter before being supplied to the motor drivers.

Position information is obtained using a precision resolver. The resolver is fed a 1600 Hz signal which is coupled into two coils mounted in quadrature. The relative amplitude of the signal in each coil is dependent upon the angular position of the resolver shaft. The two output signals are converted into digital form using a hybrid converter. The position signals are used to generate an error signal as described above and are also fed back to the Digital Processor for inclusion in the Science and Engineering data streams.

Optical isolators are used in all signal paths between the Digital Processor and Scan Drive Subsystem to maintain power bus isolation. The Converter Busy line requires transformer isolation because of its fast rise time.

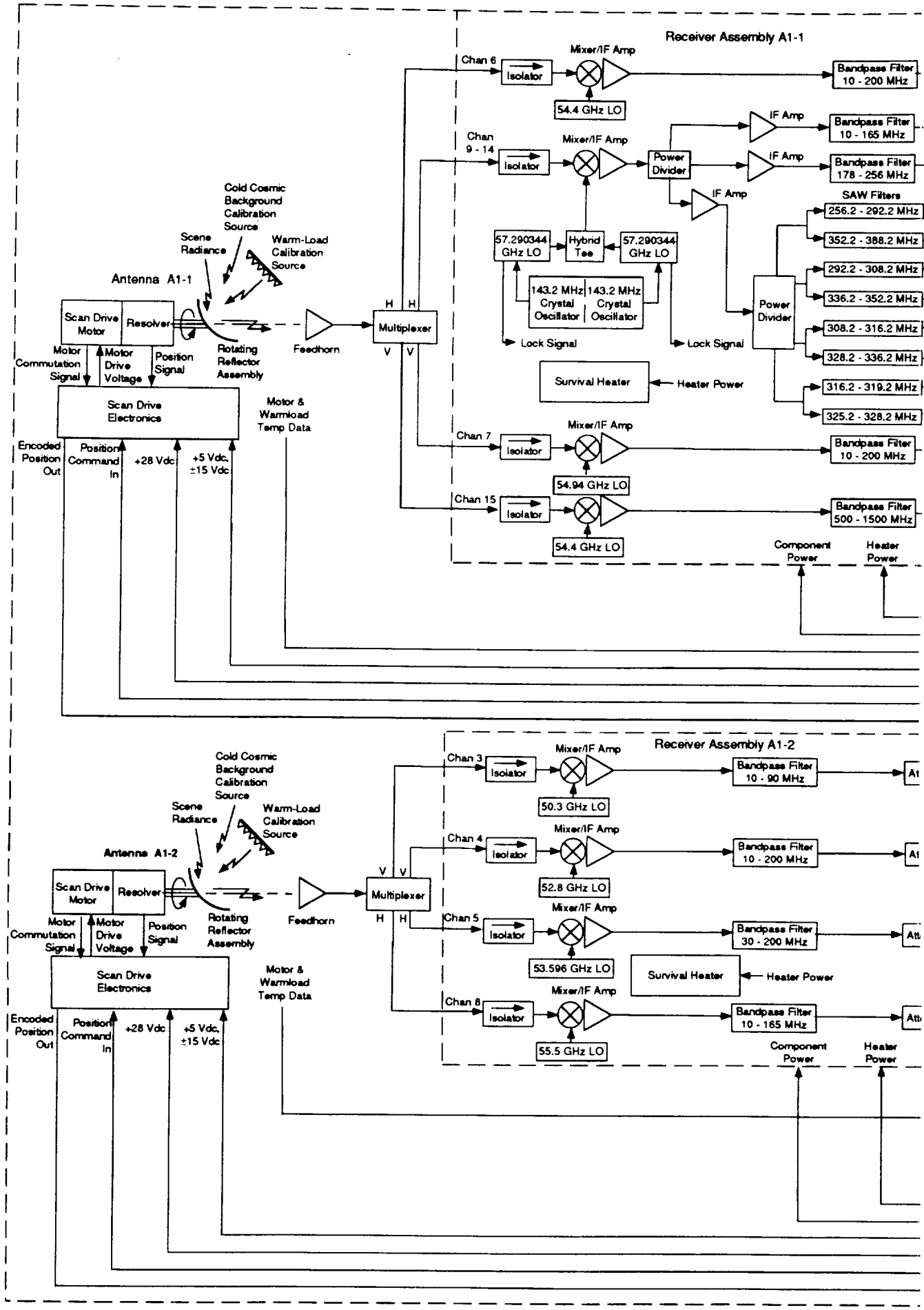
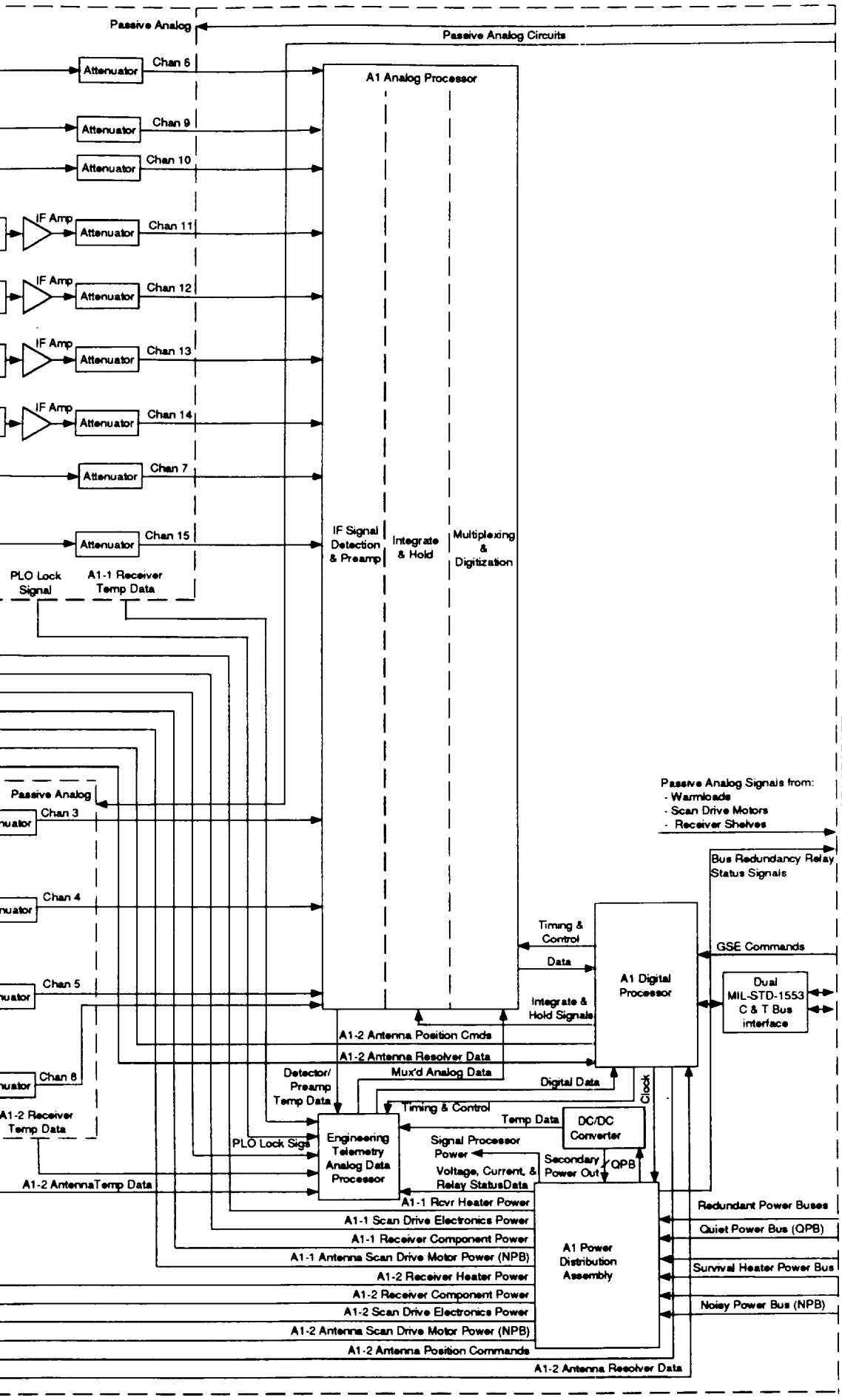


FIGURE 1 AMSU-A1 FUNCTIONAL



BLOCK DIAGRAM

FIGURE 1 AMSU-A1 FUNCTIONAL BLOCK DIAGRAM

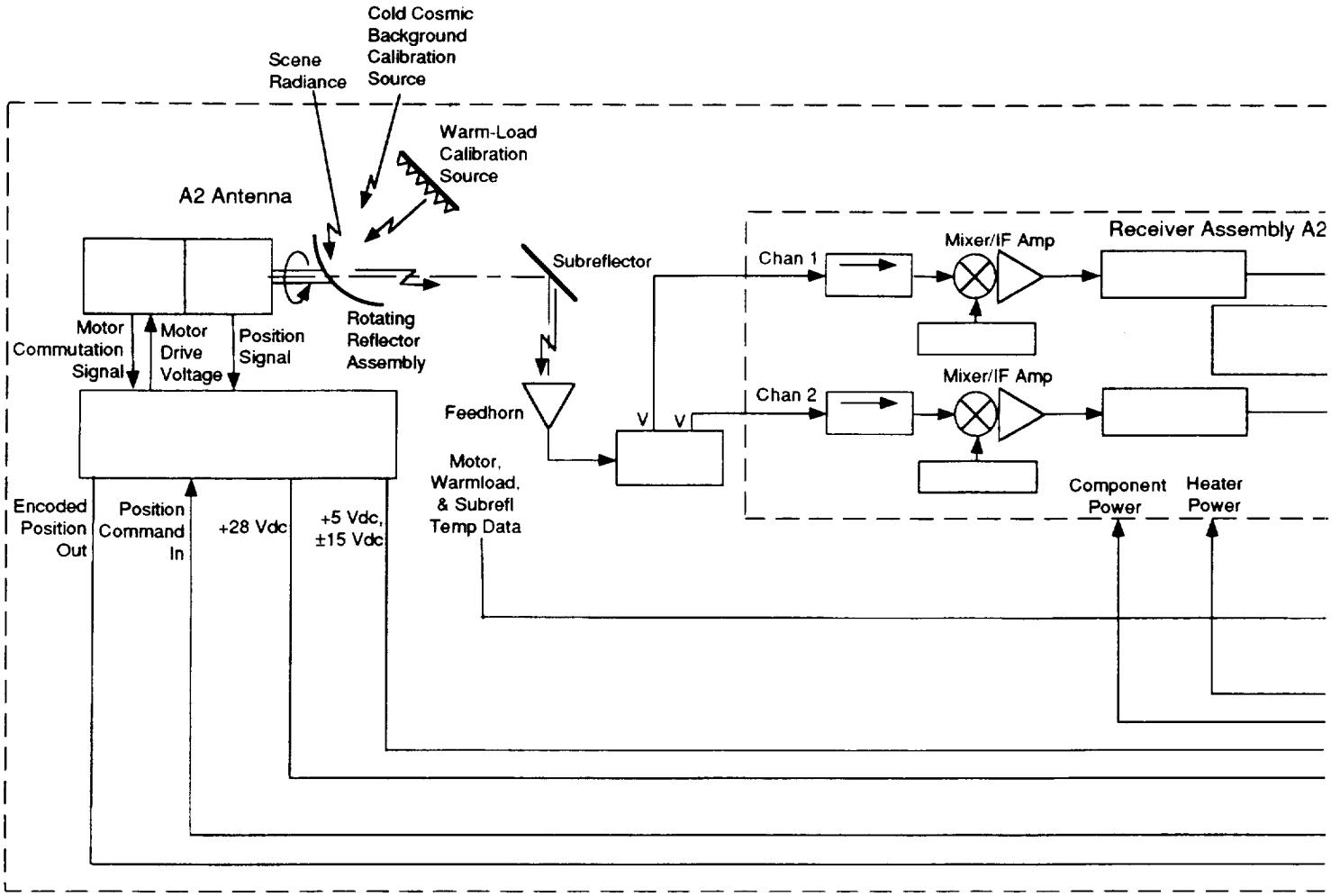
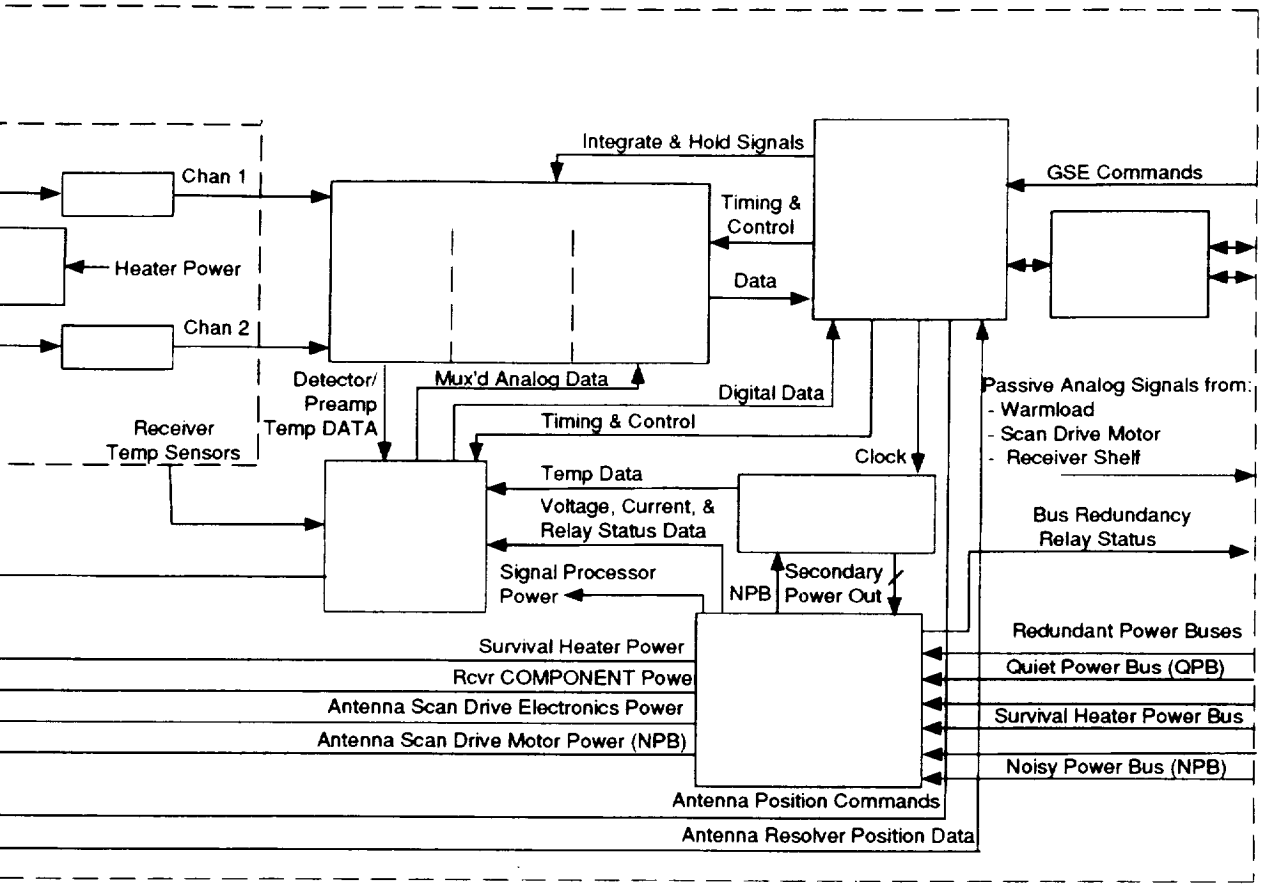


FIGURE 2 AMSU-A1 FUNCTIONAL BLO



K DIAGRAM

FIGURE 2 AMSU-A1 FUNCTIONAL BLOCK DIAGRAM

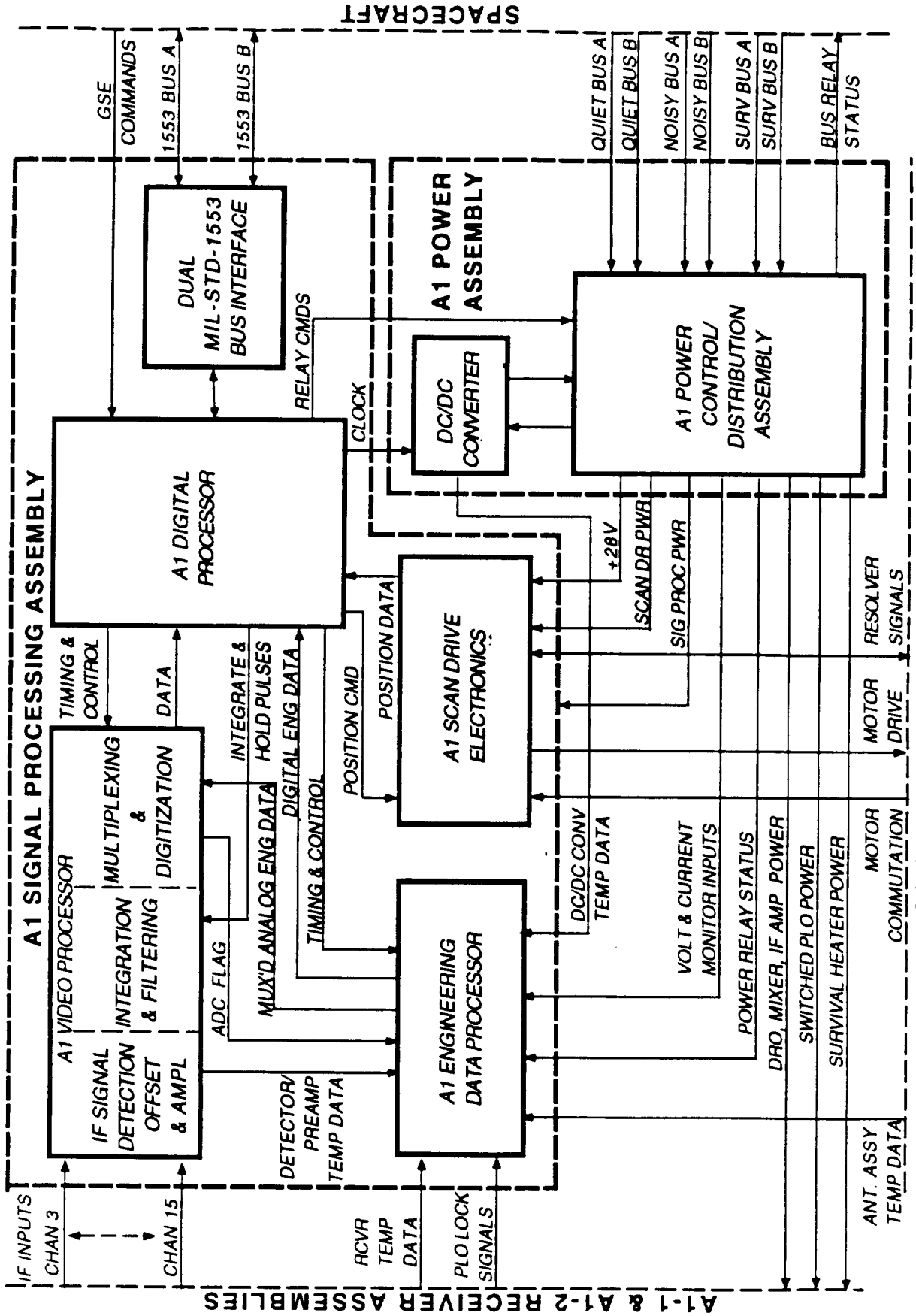


Figure 3 EOS/AMSU-A1 Signal Processor & Power Distribution Subsystem

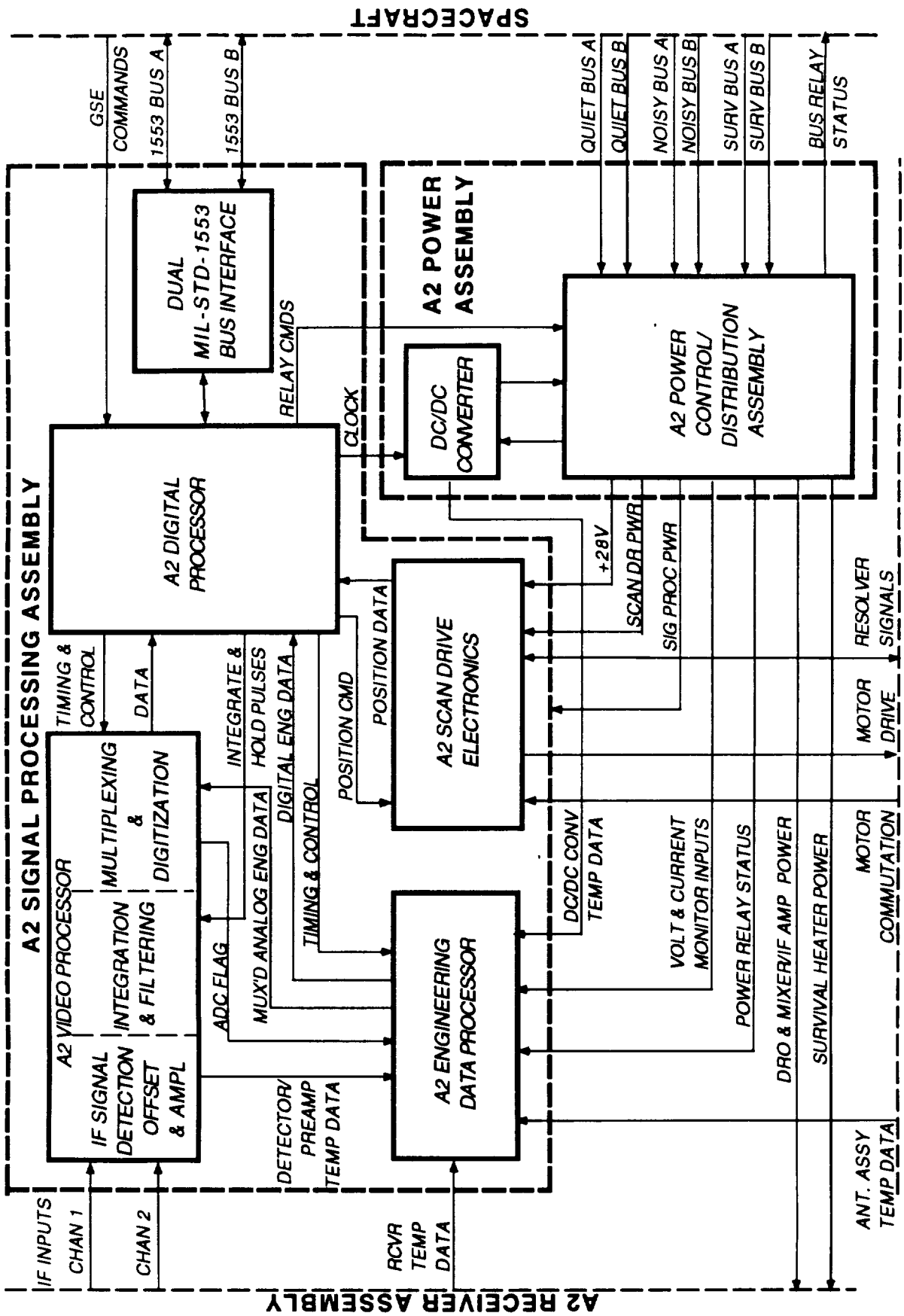


Figure 4 EOS/AMSU-A2 Signal Processor & Power Distribution Subsysem

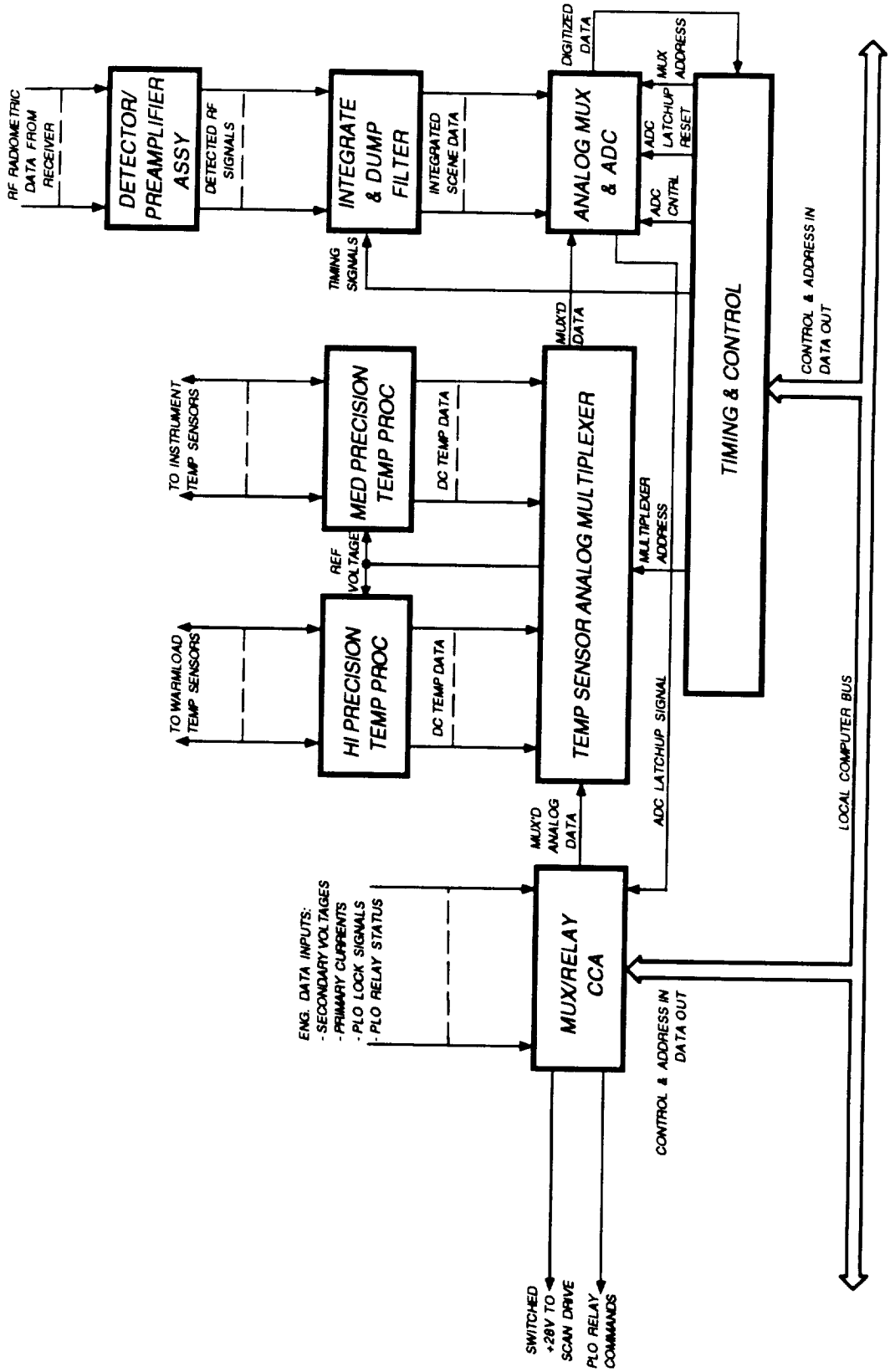


Figure 5 Analog Processor Block Diagram

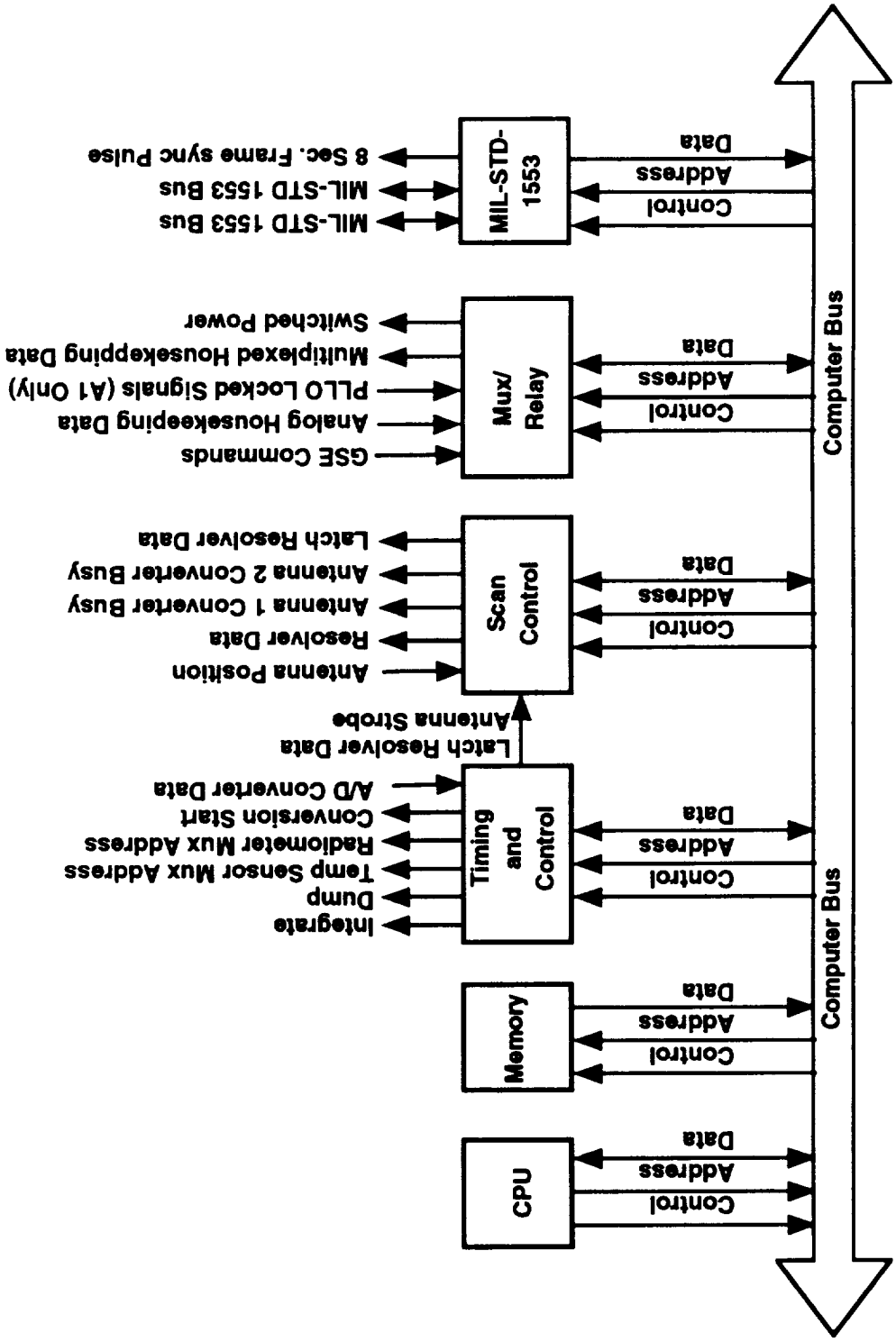


Figure 6 Block Diagram EOS/AMSU Digital Signal Processor

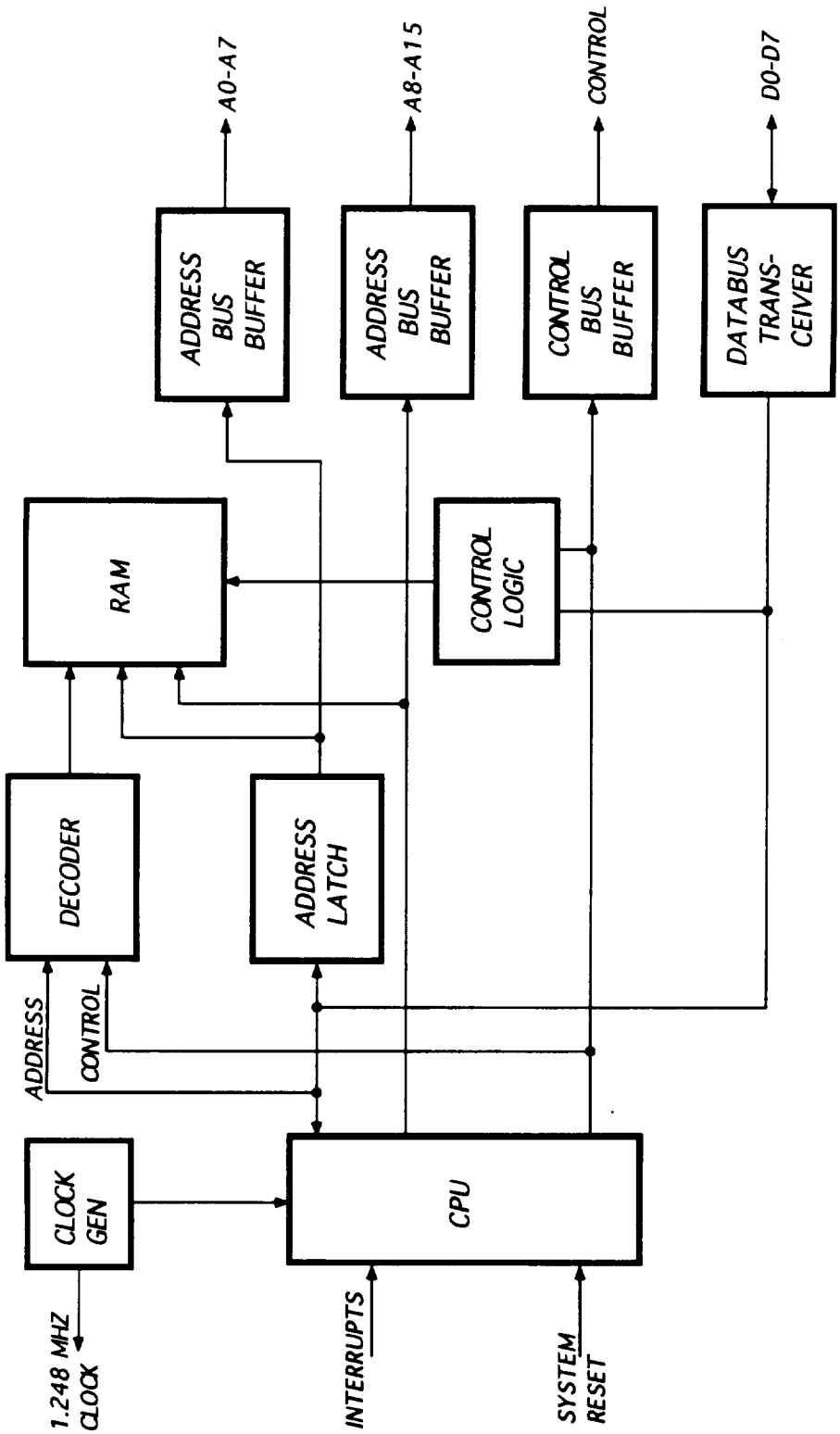


Figure 7 CPU Block Diagram

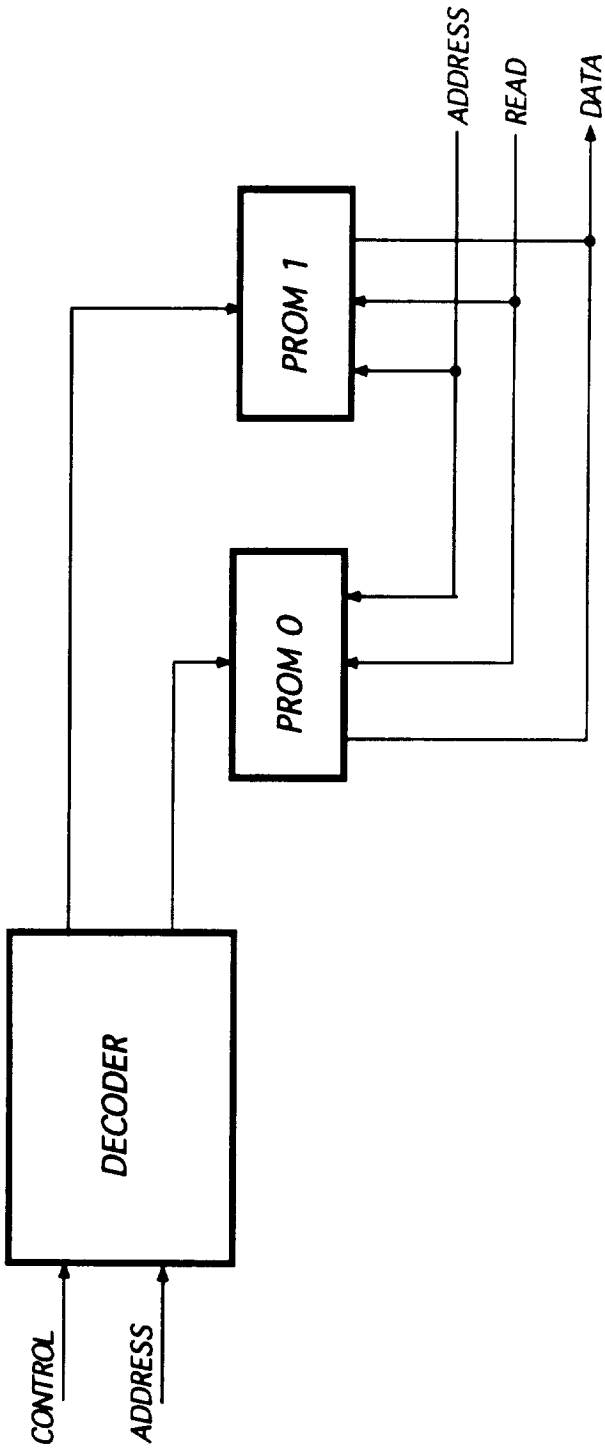


Figure 8 Memory Block Diagram

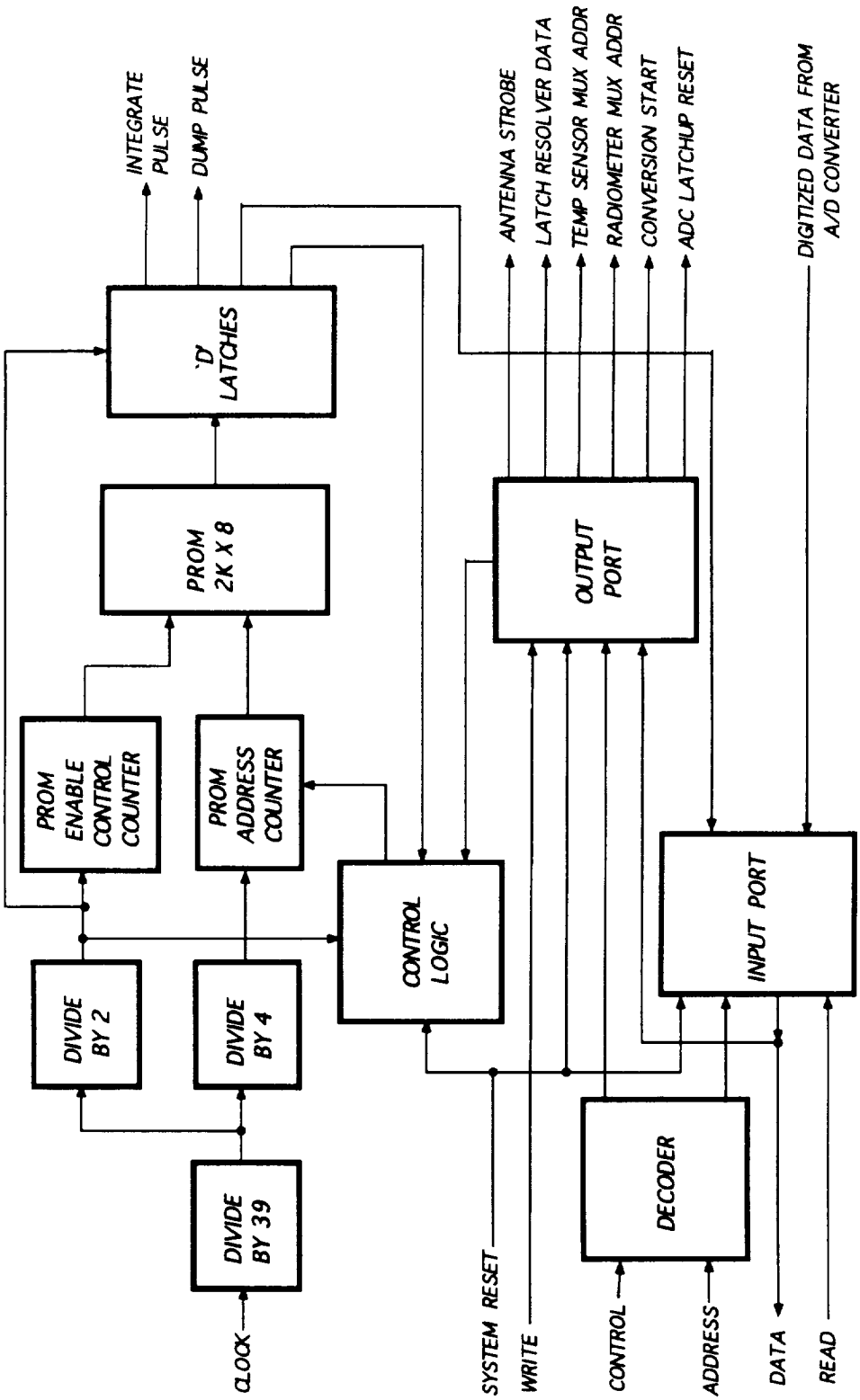


Figure 9 Timing and Control Block Diagram

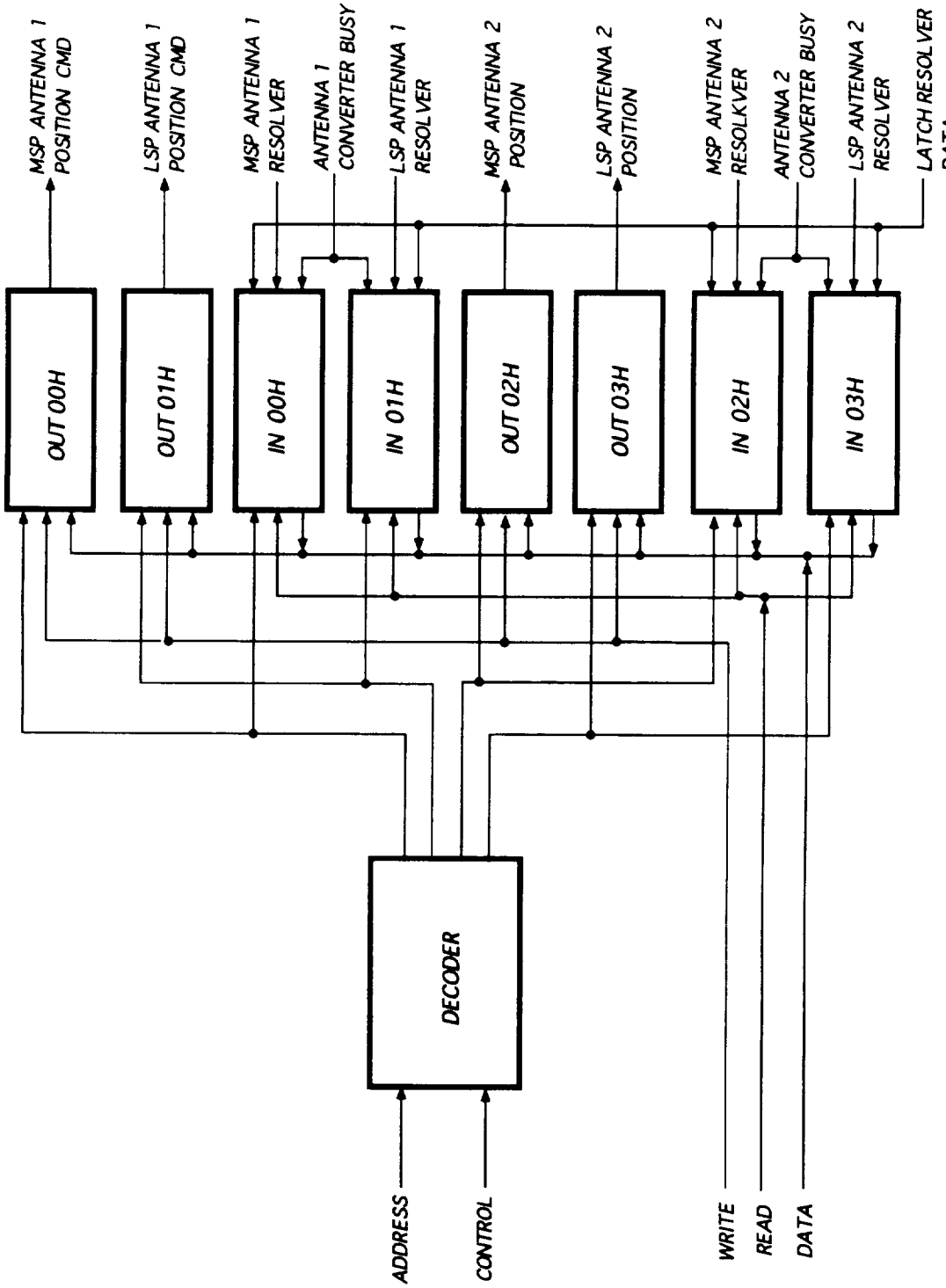


Figure 10 Scan Control Interface Block Diagram

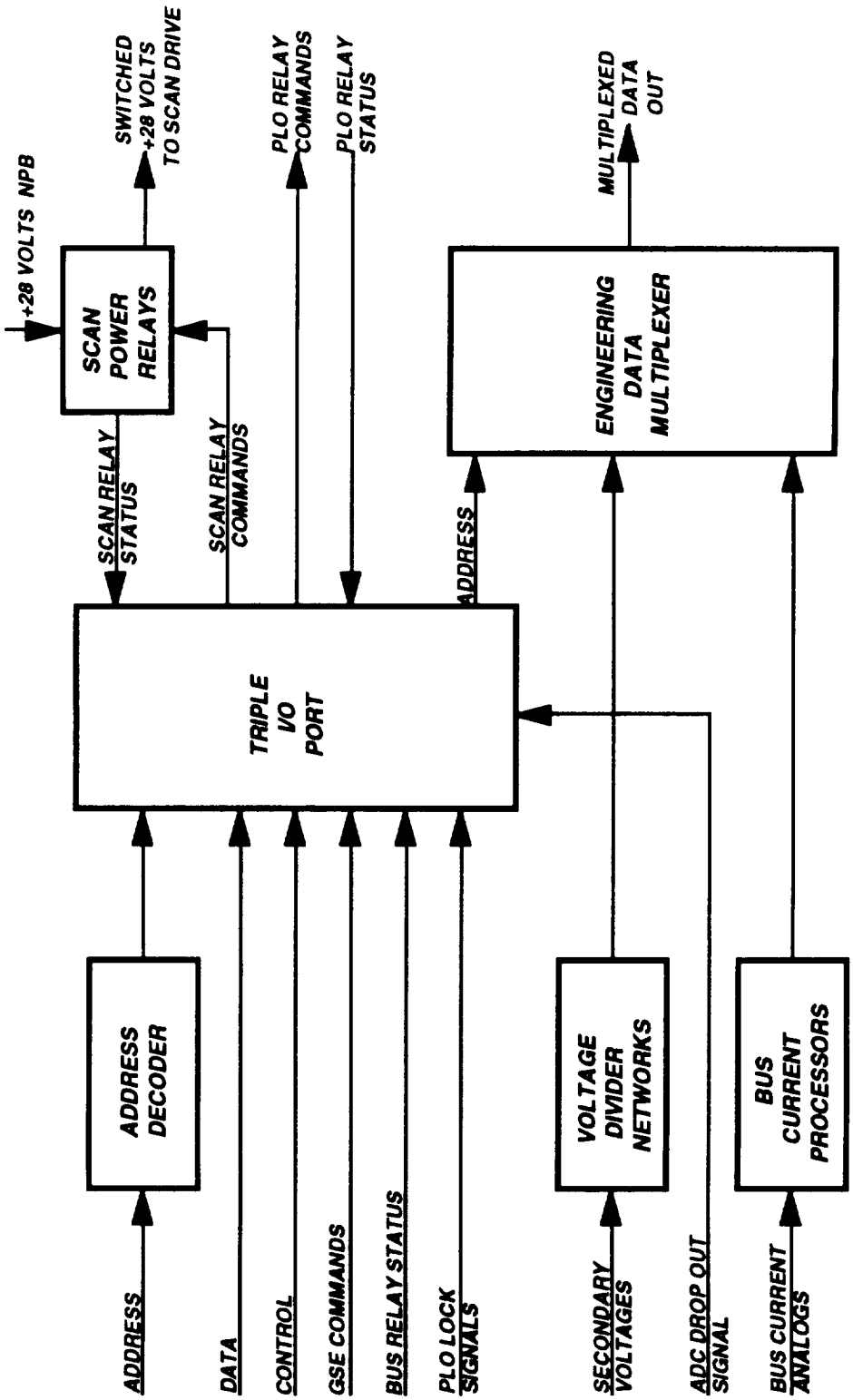


Figure 11 Mux/Relay Block Diagram

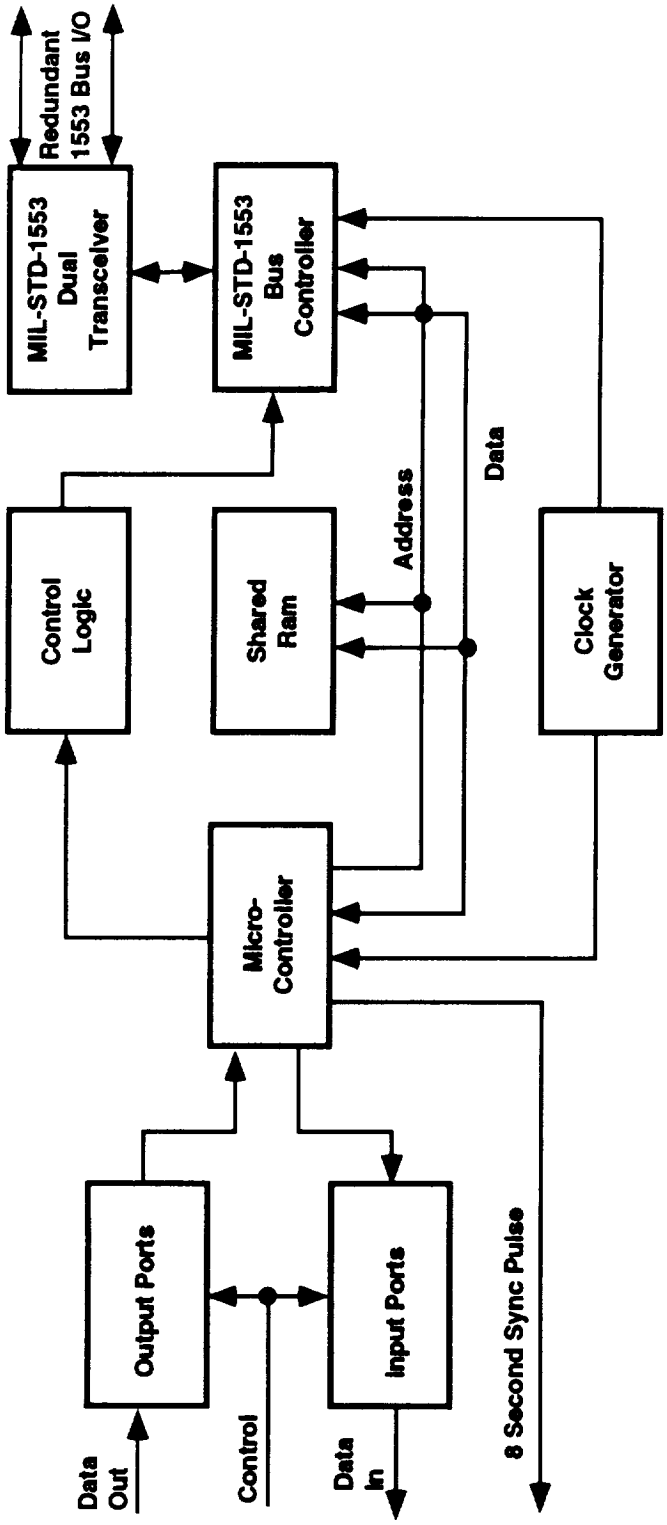


Figure 12 Block Diagram MIL-STD-1553B Interface

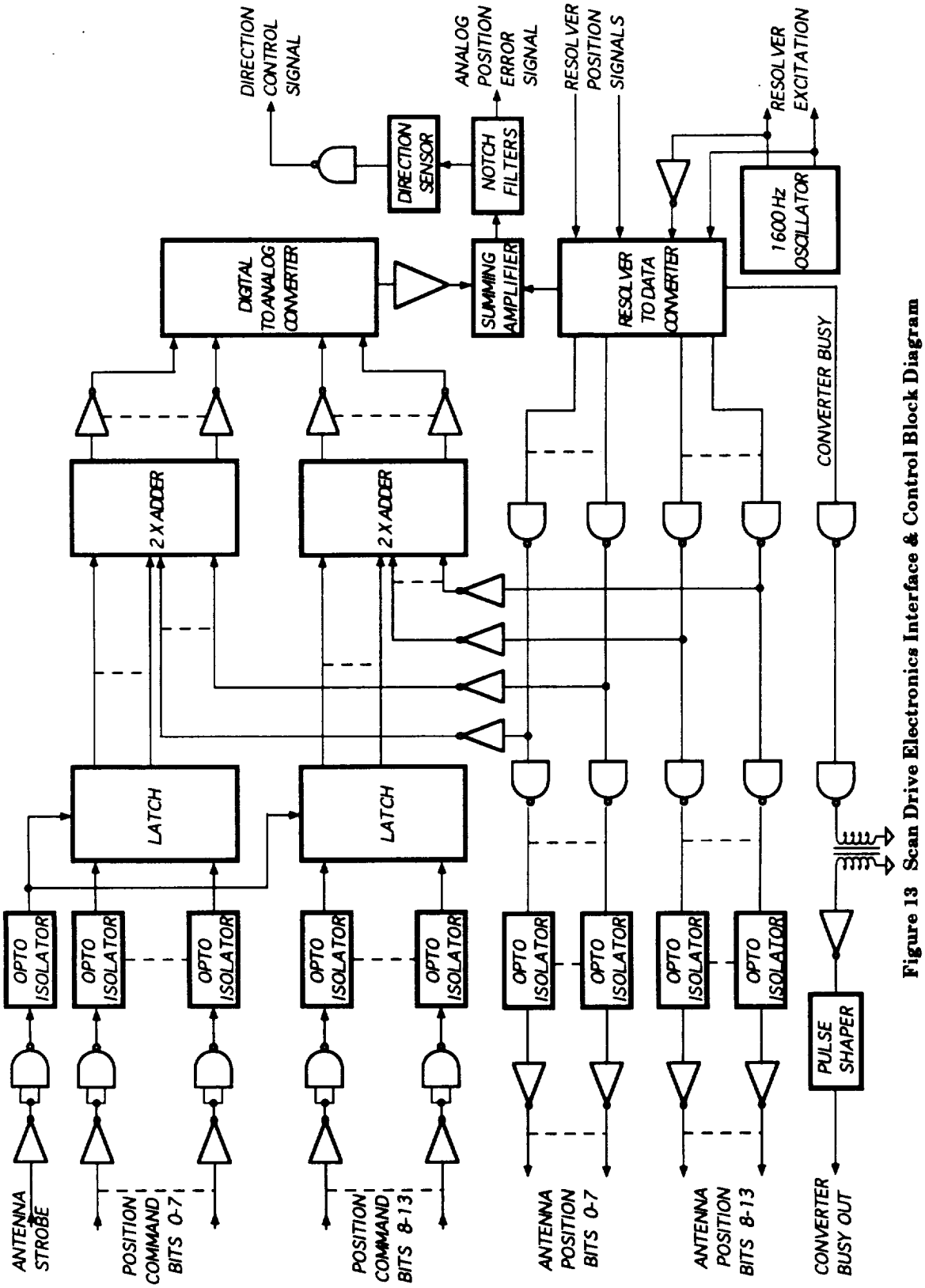


Figure 13 Scan Drive Electronics Interface & Control Block Diagram

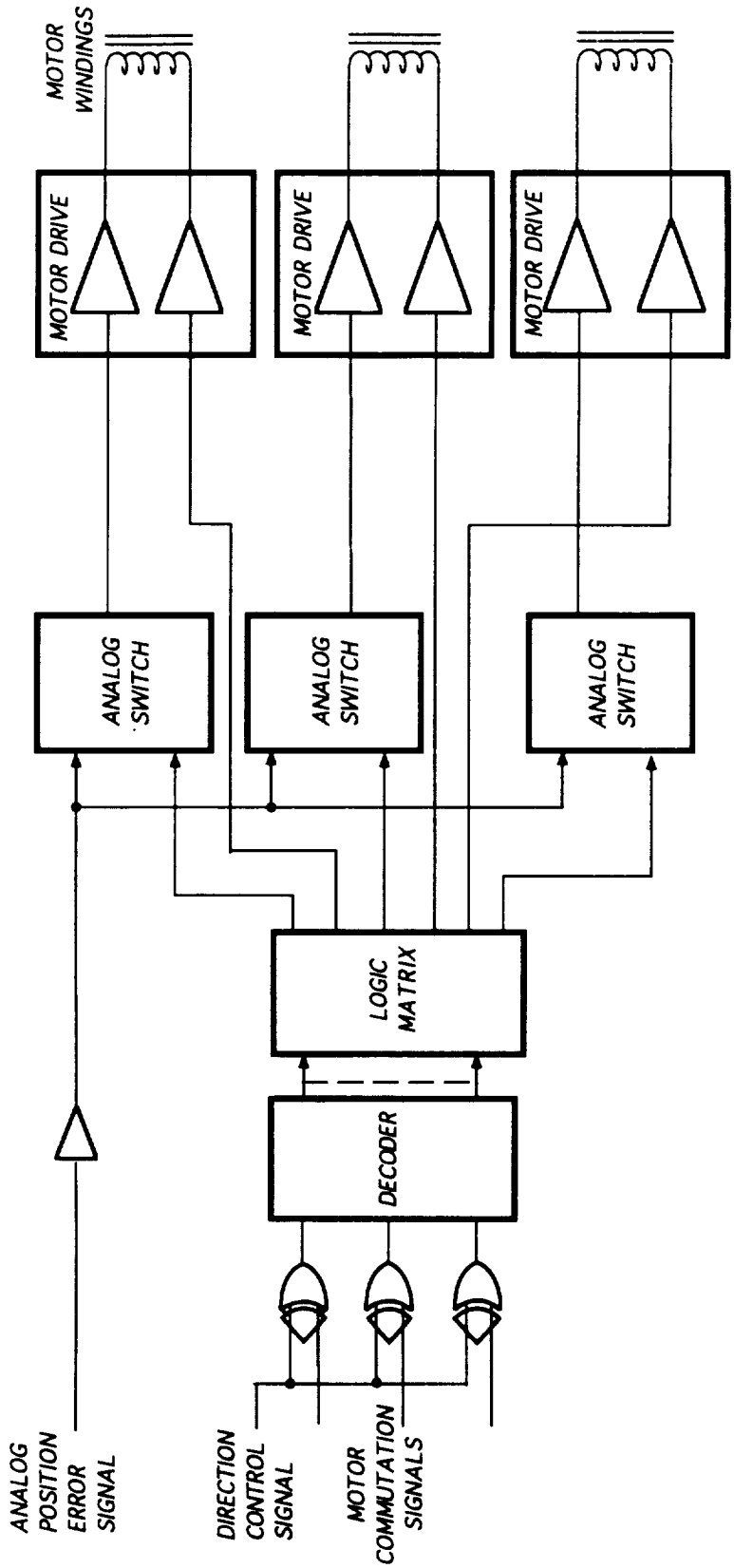


Figure 14 Scan Drive Output Block Diagram

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16. ABSTRACT (*Maximum 200 words*)

This document consists of a set of block diagrams and internal logic diagrams that show the signal inputs, outputs, and internal signal flow.

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